Module Introduction

- **PURPOSE:**
  This module, MC68000 and MC683xx Overview, provides an overview of the Freescale modular, embedded processor families based on the MC68K core.

- **OBJECTIVES:**
  - Describe the history of the 68K microprocessor.
  - Identify common associated features of the MC68300 family.

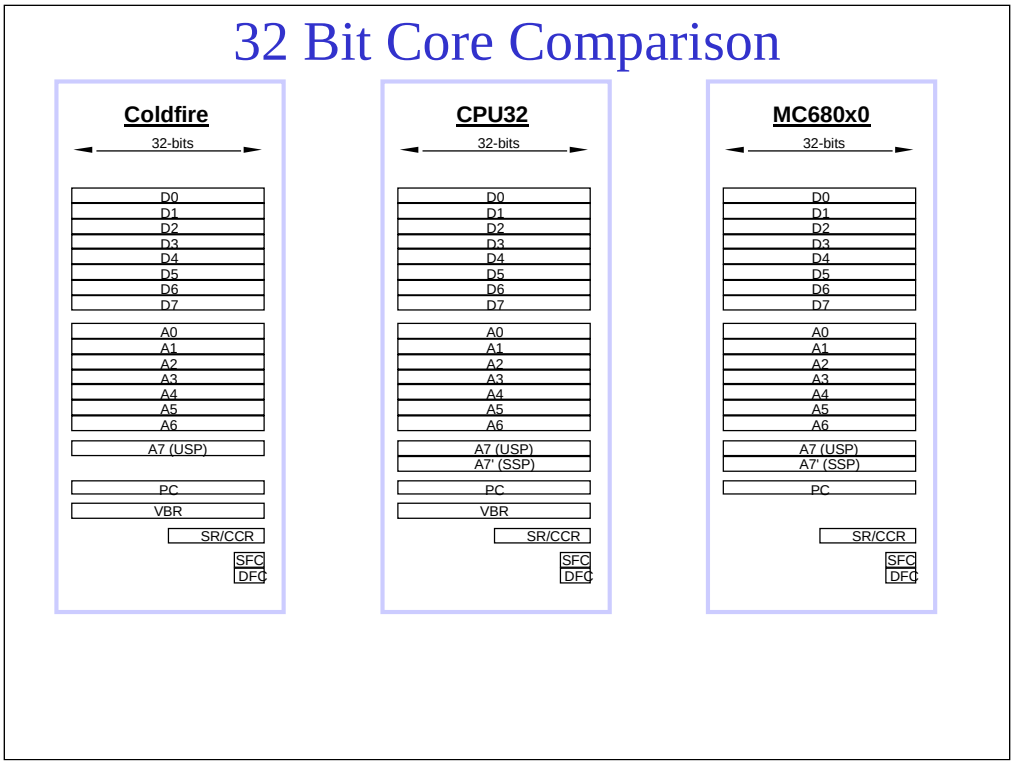
- **CONTENT:**
  - 19 pages
  - 4 questions

- **LEARNING TIME:**
  - 30 minutes

This module is an overview of the 68000 and 68300 families. It provides an overview of the modular, embedded processor families based on the MC68K core. It will describe the register set common to each of the CPUs, the context switching model and interrupt structure used by the software to implement a design. Common hardware features of the MC68300 family will also be discussed.

After taking this module you will be better able to describe where the 68K families came from; identify common features such as the InterModule Bus (IMB). Also, you'll be able to identify common IMB peripheral modules such as the system integration module (SIM), serial modules, timer modules, and Background Debug Mode (BDM).

Although there is no prerequisite for this module, some experience with modular, embedded processor families based on the MC68K core would be an asset.



The MC68000 architecture was introduced in the late 1970s. The programming model contains eight data registers, D0 –D7, and seven Address Registers, A0 – A6. Two registers, A7 and A7', are stack pointers.

A Vector Base Register (VBR) was added when the CPU32 was introduced in the early 1980s. The Vector Base Register (VBR) defines the starting address of the exception vector memory block, allowing it to relocate this block for various tasks.

The Coldfire programming model, a variable length Reduced Instruction Set Architecture, was introduced in the early 1990s. Only one stack pointer was retained.

68K Microprocessor History

The 68K family of microprocessors has been on the market since 1979, with the introduction of the MC68000 line. This was Motorola's first 32-bit microprocessor, capable of performing 2 million calculations per second. This device was used in scientific, data processing, and business applications. Since 1979, there have been significant improvements in functionality, speed, performance and third-party support of 68K. With the introduction of the 68020, 68040 and 68060 lines, Motorola took its processors into the 1990's as one of the world's market leaders. These devices still constitute a large percentage of Motorola's microprocessor market share. The 68K microprocessor, while originally targeted for the computer market, was recognized as being more suited to embedded processor applications where price and performance were required in high volumes at low cost..

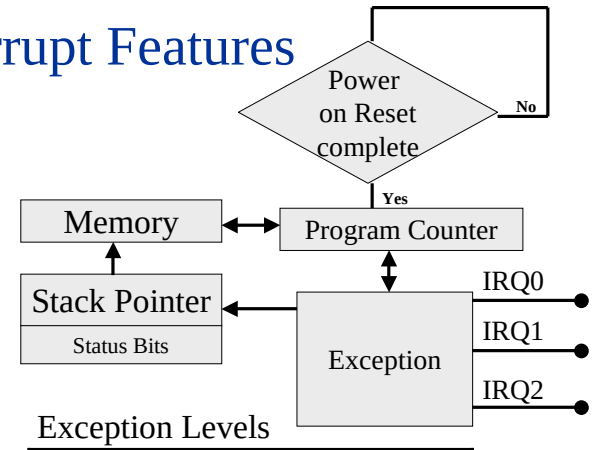
Motorola introduced a more stream-lined architecture,the 68300 family, that was specifically targeted to the embedded market, with on-chip peripherals and lower prices than the 68K processors. To compete in the embedded market place, the geometry, instruction set, and price had to be reduced. Thus, with a history of robust peripherals, the 68K legacy evolved in to a new family of processors named ColdFire, a variable length reduced instruction set architecture CPU.

The ColdFire family provided a migration path from the 68K microprocessor family in the mid-1990's. The 68K family is a much loved line of processors and sales continue to be substantial. The applications that The 68K microprocessor's applications are designed to have long life-spans and customers want to retain their investment in this family of processors. Today, a customer can purchase a two MIP MC68000 or a Coldfire four hundred MIP machine that has the same software model.

[Reference info for previous page]

Interrupt Features

- **Exception Processing**
  - Caused by an Interrupt
  - Uses the stack pointer to store machine status and other data
  - Loads the Program Counter with a new value
- **Seven levels of interrupt priority**
  - Level 7 Non-Maskable
  - Levels 1-6 Maskable
- **3-Bit Mask in CCR**
  - Determines Lowest Interrupt Priority Level allowed
- **200 unique interrupting sources allowed**
  - User Defined
- **7 Auto-Vectors**
  - One per interrupt level



Exception Levels

	IRQ2	IRQ1	IRQ0
Level 1	**0**	**0**	**x**
Level 2	**0**	**1**	**0**
Level 3	**0**	**1**	**1**
Level 4	**1**	**0**	**0**
Level 5	**1**	**0**	**1**
Level 6	**1**	**1**	**0**
Level 7	**1**	**1**	**1**

The MC68000, CPU32 and Coldfire CPUs operate in base mode once the power-on/reset sequence has been completed.

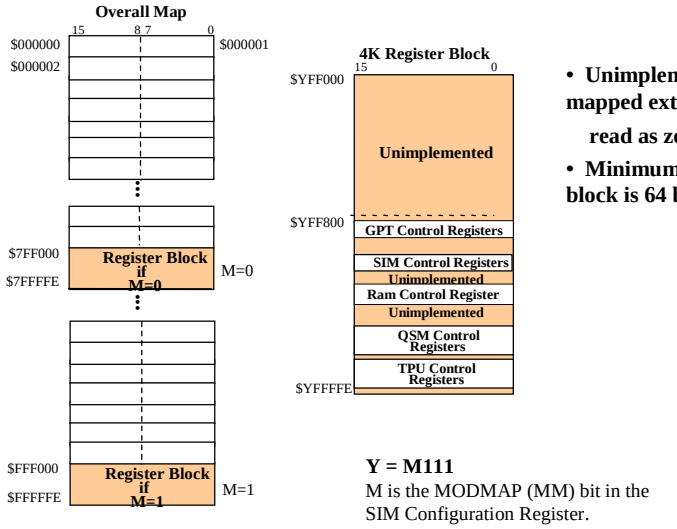
It begins executing instructions fetched from the memory location specified in the Program Counter (PC). A software or hardware generated signal called an exception, can cause the processor to discontinue fetching instructions using the Program Counter.

When an exception occurs, a hardware algorithm is implemented that cause various status bits and other data in the machine to be stored using the stack pointer to store the values in the memory locations specified by the Stack Pointer. A new value is placed in the Program counter based on the cause of the exception. The CPU then resumes fetching and executing instructions using the new value in the program counter.

A subset of exceptions are caused by three external pins, IRQ0-2. These pins can cause seven levels of hardware interrupt. The highest level interrupt, Level 7, is non-maskable. The remaining six levels of interrupt are maskable or allowed by the software via the 3 bit mask in the Condition Code Register (CCR). The value of the mask bits determines the lowest level of allowed interrupt. As an example, if the three bit field were set to 110 or 6 (hex) then only levels six and seven could cause an exception. If the three bit field were set to 111 or 7 (hex), only the non-maskable level 7 could cause an exception.

As mentioned earlier, an algorithm determines how the Program Counter is to be loaded when an exception occurs. For the three IRQ pins, there are two tables of entries that the hardware can use to load the Program Counter when an exception occurs. The default path has 200 unique table entries that the user defines. If the external pin AVEC* and the IRQ pins are asserted concurrently, then a table containing seven entries, one for each level of interrupt is used.

MC68300 family Memory Map



- **Unimplemented Blocks are mapped externally.**

  read as zeros (writes have no effect).
- **Minimum size of a Module's control block is 64 bytes.**

Y = M111
M is the MODMAP (MM) bit in the SIM Configuration Register.

- **Unused locations within a Module's control block are read as zeros (writes have no effect).**

The MC68300 family memory map has an address range of $0 to $FFFFFF or 16 Megabytes. The control registers for the peripherals in an MC68300 product reside in 4K (hex) bytes that can be located in the middle of the memory map or at the end of the memory map.

If the value of the MODMAP (MM) bit in a register of the System Integration Module is zero the starting address will begin at $7FF000.

If the value of the MODMAP (MM) bit in a register of the System Integration Module is one the starting address of the control register block is $FFF000.

Question

If all the mask bits in the MC68300 Condition Code Register are zero, how many levels of interrupt can be generated by the IRQ pins? Click on your choice and click Done.

a) 0

b) 1

c) 3

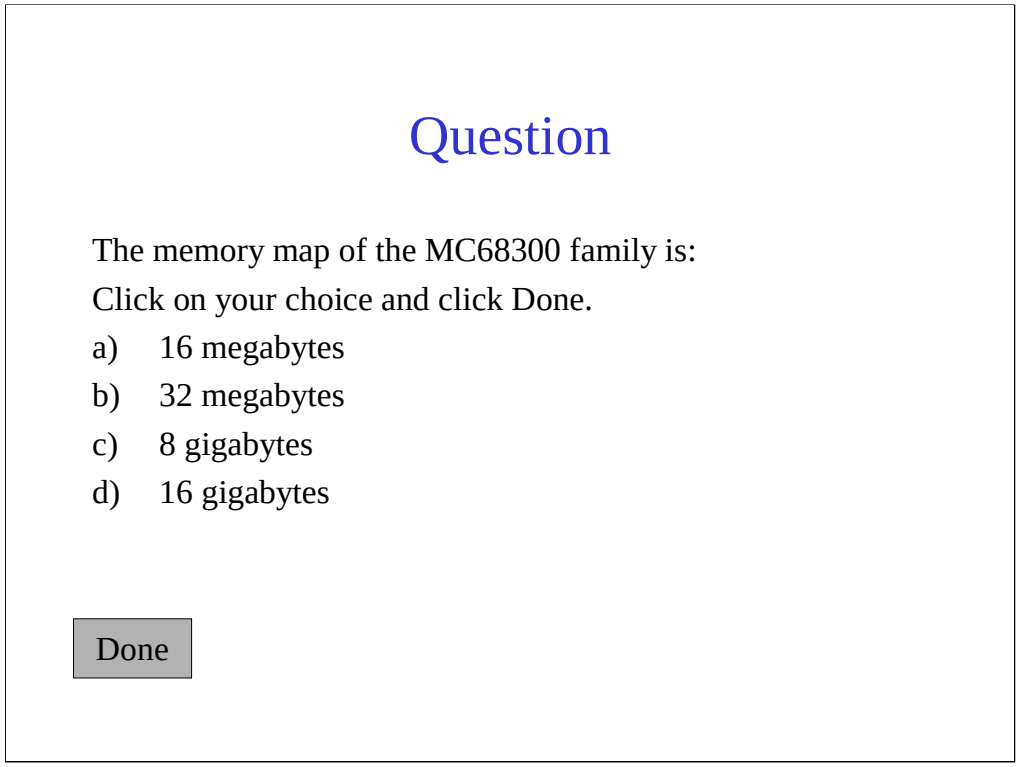
d) 7

Done

Here are a couple of questions on the material covered to this point.

Answer:

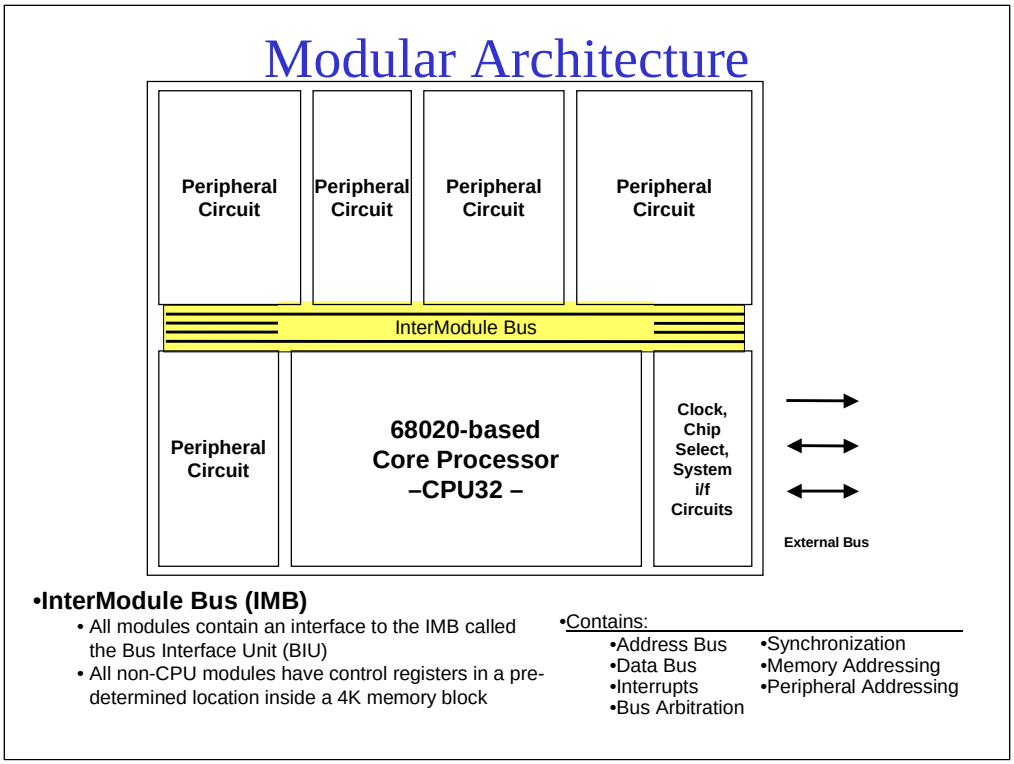
The highest level interrupt, Level 7, is non-maskable. The remaining six levels of interrupt are maskable or allowed by the software via the 3 bit mask in the Condition Code Register (CCR). The value of the mask bits determines the lowest level of allowed interrupt. Therefore since they are all zero all seven levels of interrupt are available.



Here's a question for you.

Answer:

The MC68300 family memory map has an address range of $0 to $FFFFFF or 16 Megabytes.

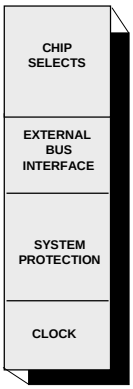


A representation of the MC68300 family silicon floor plan is shown here. The CPU32 Core Processor, various peripheral blocks and the external bus all connect to the InterModule Bus or Silicon Backplane.

The InterModule Bus (IMB) contains the address and data buses, interrupt, bus arbitration, synchronization, and handshaking lines. All modules contain a standard Bus Interface Unit (BIU) connection to the IMB. The control registers for each of the non-CPU modules reside in a predetermined location inside a 4K (Hex) memory block. Each of the MC68300 family members have a System Integration Module or equivalent that interfaces the InterModule Bus with the External Bus.

SIM Overview and Features

- 12 Independently Programmable Chip Selects
  - Software Selectable (2K to 1M)
  - Up to 13 programmable wait states
  - Built-in CSBOOT
- External Bus Interface
  - Dynamically Sized Data Bus
- Hardware Watchdog System
  - Software Watchdog Timer (COP)
  - Periodic Interrupt Timer
  - Bus Response Timer Monitor
- Up To 22 Independent Parallel I/O Pins
  - 15 Bi-directional, 7 Output Only
- Programmable on-chip Phase Lock Loop for system clock
  - Up to 25MHz operation from 32.768 KHz crystal



Next, let's look at the System Integration Module (SIM). This module allows a glueless external peripheral and memory interface.

The SIM consists of 12 independently programmable Chip Selects with a software selectable block size from 2K bytes to 1 Megabyte and up to 13 programmable wait states. There is a built in CSBOOT chip select for use when coming out of Power-On/Reset.

The External Bus Interface (EBI) has a dynamically bus sized 16 bit data bus, a 24 bit Address bus and control signals.

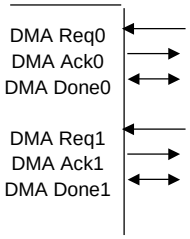
System Protection features include a Software Watchdog Timer, Periodic Interrupt Timer and Bus Timeout function.

The SIM contains up to 22 independent parallel I/O pins. Fifteen of these pins are designated as bi-directional, whereas seven are output only.

The programmable on-chip Phase Locked Loop (PLL) clock system makes it possible to achieve any clock rate up to 25 MHz from a simple, inexpensive 32.768 kHz crystal. The PLL's operating frequency is programmable via a memory-mapped register and enables clock rate changes during design or operation.

Direct Memory Access (DMA) Control Module

- Two Independent DMA Channels
- Single *fly-by* or Dual Address Transfers
- Full 32-bit:
  - Address Pointers
  - Transfer Counters
  - Data Size
- Source and Destination Data Sizes may be mixed
- Handshake lines for Cycle Steal or Burst
- Selectable Bus Bandwidth utilization
- Maximum Sustainable Data Transfer Rate:
  - 50 Mbytes per second (@ 25 MHz)

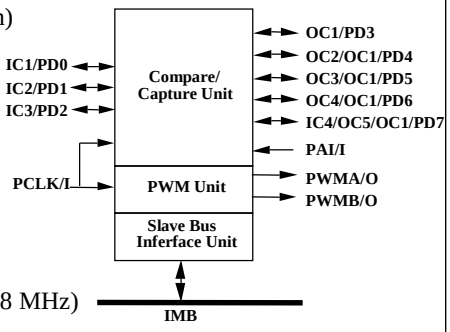


Two independent Direct Memory Access (DMA) controllers are available on some MC68300 products. Each controller has its own control pins and greatly improves data transfer rates over software-controlled methods.

These full-function DMAs are capable of byte, word and long word data transfers. Note that there are two methods of operation, cycle steal and burst. Their bus loading is programmable up to 100% bus utilization.

General Purpose Timer (GPT) Module

- **Compare/Capture Unit**
  - Three Input Capture Channels
  - Four Output Compare Channels
  - One Dual Purpose Channel (Input Capture or Output Compare)
  - One Output Compare Function Controlling Multiple Channels (**OC1**)
  - Dedicated 16-Bit Counter (240 ns Resolution)
- **Pulse Accumulator**
  - Event Counting Mode or Gated Time Accumulation
  - Dedicated Input Pin
- **Two Pulse Width Modulation Outputs**
  - Eight Bits of Resolution
  - Dedicated 16-Bit Counter
  - Frequencies from 4 Hz To 32.8 KHz (@16.78 MHz)
- **Other Features**
  - All Pins General I/O (Eight Bi-Directional Port GP)
  - Nine-Stage Prescaler
  - Dedicated Clock Input Pin



The GPT contains a Compare/Capture unit with four timer channels, a separate pulse accumulator unit and two Pulse Width Modulation Units. Three of these channels are capable of input capture, and all four can provide output compare. In addition, a PWM unit contains two separate 8-bit PWMs. Also, a separate pulse accumulator provides pulse counting and measurement.

This unit provides three input capture channels, four output compare channels, one dual purpose channel (input capture or output compare), one output compare function controlling multiple channels (OC1), and a dedicated 16-bit counter with 240 ns resolution.

This accumulator provides an event counting mode or a gated time accumulation mode via a dedicated input pin.

This unit provides two pulse width modulation outputs each having eight bits of resolution, a dedicated 16-bit counter, and output frequencies from 4 Hz To 32.8 KHz (@16.78 MHz).

The GPT module offers additional features. These include all pins general I/O (8 bi-directional port GP), a nine-stage prescaler, and a dedicated clock input pin.

Time Processing Unit (TPU) Features

- **Sixteen input/output pins — each associated with a timer channel**
- **Each channel has an event register consisting of:**
  - **—A 16-bit capture register**
  - **—A 16-bit compare/match register**
  - **—A 16-bit greater-than or equal-to comparator**
- **Each channel can be synchronized to one or both of the two 16-bit free-running Timer Count Registers.**
- **TCR1 is clocked by a 2-bit prescaler, which is clocked by the internal system clock.**
- **TCR2 is clocked either by a 2-bit prescaler (clocked by the internal system clock) or by an external clock**

The Time Processor Unit (TPU) is the main distinguishing feature of the MC68332. This module is a timer system capable of flexible and intelligent time functions. It greatly offloads the core CPU from most timing function event handling.

The TPU has sixteen I/O pins, each one associated with a timer channel.

Each channel has an event register consisting of a 16-bit capture register, a 16-bit compare/match register, and a 16-bit greater-than or equal-to comparator.

Each channel can be synchronized to one or both of the two 16-bit free-running Timer Count Registers (TCRs). More specifically, TCR1 is connected to the system clock thru a 2-bit prescaler. Whereas TCR2 is clocked either by a 2-bit prescaler on the internal system clock, or by an external clock.

TPU Features Continued

- **Resolution capability for a pin is the system clock divided by four (240 nsec at 16.67 MHz).**
- **Service request driven — host, match, capture, and link request per channel**
- **Servicing of pins is orchestrated by a realtime task scheduler – one of three priority levels programmed per pin**
- **Service is provided by a RISC-like processor.**
- **Execution unit for arithmetic calculations**
- **Factory-programmed ROM control store that contains a library of time functions, which can be allocated to any pin(s)**
- **Parameter registers (RAM) associated with each pin are used as a shared data space between TPU and CPU.**

Resolution capability for a pin is the system clock divided by four or 240 nsec at 16.67 MHz.

The TPU is service request driven. Each channel has a host, match, capture, and link request bit.

Pin servicing is orchestrated by a realtime task scheduler, based on one to three priority levels programmed per pin, and is provided by a RISC-like processor.

The TPU contains an execution unit for arithmetic calculations.

The TPU contains a factory-programmed ROM control store that contains a library of time functions, which can be allocated to any pin.

Parameter registers (RAM) associated with each channel are used as a shared data space between TPU and CPU.

TPU Time Functions

General purpose ("A" Mask) TPU functions facilitate:

- **Angle-based engine control (PMA/PMM; PSP)**
- **Stepper motor (SM) control**
- **Pulse-width modulation (PWM)**
- **Frequency measurement (PPWA)**
- **High-time accumulation (PPWA)**
- **Frequency divide/multiply (PPWA; OC)**
- **Pulse accumulator (ITC)**
- **Output compare (OC)**
- **Input capture (ITC)**
- **Digital input/output (DIO)**

Motion control ("G" Mask) TPU functions facilitate:

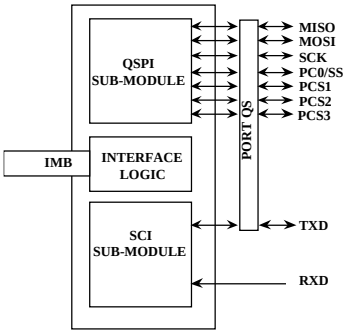
- **Queued Output Match (QOM)**
- **Fast Quadrature Decode (FQD)**
- **Multi-Phase Commutation (COMM)**
- **Input Capture/Transition Counter (ICTC)**
- **UART (UART)**
- **Programmable Timer Accumulator (PTA)**
- **Multi-Channel PWM (MCPWM)**
- **Hall Effect Decode (HALLD)**
- **Frequency Measurement (FQM)**
- **Table Stepper Motor (TSM)**

There are two choices of TPU function libraries, the "A" Mask and "G" Mask. These function libraries are microinstruction programs that reside in the control store that controls TPU facilities and effect time-related tasks.

The "A" Mask provides more classical timer functions, and the "G" Mask slants more toward motion control. . The letters "A" and "G" are found in the device part number suffix.

QSM Features

- **SCI:**
  - Enhanced Asynchronous Serial System
  - Modulus Baud Rate Counter (64 Baud to 524K Baud with 16.78 MHz Clock)
  - Parity Generation and Detection
  - Receiver Active Flag
  - True Idle Line Detect (full frame of 1's after Stop Bit Detected)
  - Ideal for remote communications
- **QSPI:**
  - Synchronous Serial Interface
  - Various Peripheral Functions Available for the Interface
    - LCD Drivers
    - EEPROM
    - A/D - D/A Converters
    - RAM
    - I/O Expansion
    - Digital Signal Processors
  - Serial Devices Appear Directly Accessible by CPU
  - Queue RAM, up to 16 transfers
  - Variable Bit (8 thru 16) Transfer Lengths
  - Automatic Chip Selects (4)
  - Programmable Delays between and during transfer
  - Master or Slave operation
  - Wraparound Mode for continuous operation



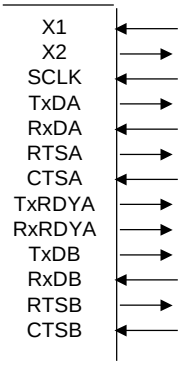
The Queued Serial Module (QSM) contains two independent serial functions, a Universal Asynchronous Receiver Transmitter (UART), sometimes called the SCI, and an enhanced Serial Peripheral Interface. The UART is a standard communications module, capable of asynchronous communications with such features as idle line detection and parity.

The SPI is a simple high-speed serial shift-register-based module that allows simple connection to a variety of peripheral functions such as A/D converters, display controllers, other processors with an SPI, and serial EEPROMs.

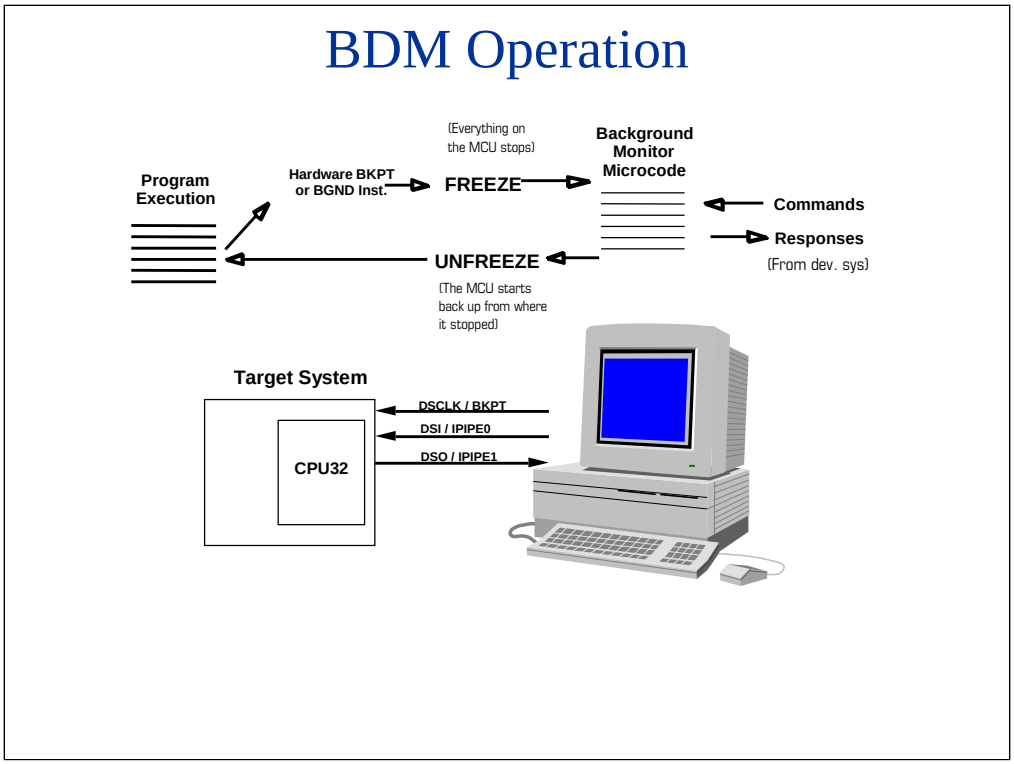
The QSPI contains a queue of 16 words to be sent or received, greatly reducing the amount of service required. Unlike other SPI modules, it can be programmed for variable length transfers, even within the queue. Roll your mouse pointer over QSPI for more information about its features and functions.

MPU Serial I/O module

- Powerful Serial I/O Module providing:
  - 2 Independent Full-Duplex Synchronous or Asynchronous Receiver/Transmitter Channels
  - Individual Baud Rate Generator
  - Select up to 76.8K baud, 1x, or 16x for R or T
  - Programmable 5-8 data bits, parity, stop bits
  - Modem Control
  - Auto Echo, Local & Remote Loopback
  - Error Detection & Interrupt Control
  - Quadruple buffered receivers
  - Double buffered transmitters



The MPU Serial I/O module contains two independent UART functions. Each function is capable of both asynchronous or synchronous communication. Each has a quadruple-buffered receiver, double-buffered transmitter and programmable data lengths.



One of the most popular features introduced in the MC68300 family is the Background Debug Mode (BDM), a feature that continues to improve in subsequent families.

In BDM, Breakpoint (BKPT), IPIPE0 and IPIPE1 pins become a serial interface to send debug commands and receive data from the MPU.

BKPT becomes the serial clock.

IPIPE0 becomes the input from the development system.

IPIPE1 becomes the output to the development system**.**

The BDM permits an external BKPT signal or the BGND instruction to freeze CPU operation and turn control over to a host connected to a serial interface, which permits economical debug hardware and system access without the need for special connections and expensive emulators.

Question

How many Input Capture Channels does the General Purpose Timer have? Click on your choice and click Done.

a) 1
b) 2
c) 3
d) 4

Done

Let’s complete this module with a couple of questions.

Answer:

The General Purpose Timer contains a Compare/Capture unit with four timer channels, a separate pulse accumulator unit and two Pulse width Modulation Units. Three of these channels are capable of input capture, and all four can provide output compare.

Question

Which of the following TPU functions are associated with the Motion Control or “G” Mask? Click on your choice and click Done.

Queued Output Match (QOM)
Programmable Timer Accumulator (PTA)
Input Capture/Transition counter (ITC)
Output Compare (PSP)

Done

Here is another question for you.

Answer:

The first two TPU functions are associated with the Motion Control or “G” Mask. The other two selections are associated with the General Purpose or “A” Mask.

Module Summary

- 68K Microprocessor history
- Modular architecture
- Bus timing and control
- SIM overview
- MPU timer module features
- TPU features
- QSM features

Let’s review the 68000 and 68300 Overview module. First, we looked at a brief history of our 68K microprocessor and the necessary implementation of the ColdFire processor product line. Then, we looked at basic modular architecture and its inclusive components. Finally, we took a closer look at these components and their unique features and functions. This information should provide you with a baseline of knowledge related to the 68K microprocessor family.